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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/041,144	01/04/2002	Kazuo Ishimoto	81784.0247	2423

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EXAMINER	
AGGARWAL, YOGESH K	
ART UNIT	**PAPER NUMBER**
2615	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/041,144	ISHIMOTO ET AL.	
	Examiner	Art Unit	
	Yogesh K. Aggarwal	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments filed 06/03/2005 have been fully considered but they are not persuasive.

Examiner's response:

2. Applicant argues with respect to claims 1-10 that information charges generated in odd and even lines during a first period A are respectively accumulated, and the information charges generated in an odd line are compounded into the information charges generated in an even line. With this, information charges in the odd line results in G (2A), while information charges in the even line result in zero. During a following second period B, information charges are further accumulated in the odd and even lines, respectively. With this, information charges in the odd line result in G (2A +B), while information charges in the even line result in G (B). **The Examiner respectfully disagrees.**

3. In Hamasaki (US Patent # 5,990,952) information charges generated in photodiodes of odd and even lines during the first period A are respectively accumulated, and then mixed in a vertical register, whereby main information charge Q1+Q2= G (2A) is obtained as agreed by the applicant. During a second period B, Q1'+Q2'= G (2B) is obtained. Examiner notes that the claim broadly recites "accumulating information charges generated in a light receiving pixel in each odd line during a second period in the portions of vertical shift registers corresponding to each odd line, and of accumulating information charges generated in a light receiving pixel in each even line during the second period in the portions of vertical shift registers corresponding to each even line in addition to the information charges that are already accumulated therein". Therefore the claim is interpreted to mean that the charges G (2A) and G (2B) being accumulated

in a vertical shift register which may be different stages of the vertical shift register. The claim does not explicitly recite "...information charges that are already accumulated therein **in the same stage of the vertical shift registers**". Therefore in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., During a following second period B, information charges are further accumulated in the odd and even lines, the odd line result in G (2A +B), while information charges in the even line result in G (B)) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamasaki (US Patent # 5,990,952) in view of Murayama et al. (US Patent # 4,686,573).

[Claims 1and 4]

Hamasaki teaches a method for driving a solid state imaging device (figure 1) comprising accumulating information charges generated in a plurality of light receiving pixels (figure 1, sensor 1) during a first period in portions of vertical shift registers (2) corresponding to each odd line and in portions of vertical shift registers corresponding to each even line (col. 4 lines 20-41,

figure 2), vertically transferring the information charges (figure 4A, charge Q1 and Q2) accumulated in the portions of vertical shift registers (2) corresponding to each odd line to the portions of vertical shift registers corresponding to each adjacent even line, compounding the information charges (Q1 + Q2) originated from the portions of vertical shift registers corresponding to each odd line into the information charges accumulated in the portions of vertical shift registers corresponding to each adjacent even line, and holding resultant information charges in the portions of vertical shift registers corresponding to each even line (col. 4 lines 41- 67, Col. 5 lines 22-28, figures 4A, 4B and 4C),

accumulating information charges generated in a light receiving pixel in each odd line (Q1`) during a second period (figure 3 shows short exposure time) in the portions of vertical shift registers (2) corresponding to each odd line, and of accumulating information charges generated in a light receiving pixel in each even line (Q2`) during the second period in the portions of vertical shift registers corresponding to each even line in addition to the information charges that are already accumulated therein (col. 4 line 67- col. 5 line 21, col. 5 lines 29-30, figures 4A-4D); transferring the information charges accumulated in the portions of vertical shift registers corresponding to each odd line and the information charges accumulated in the portions of vertical shift registers corresponding to each even line to a horizontal shift registers (col. 6 lines 25-37).

Hamasaki teaches that the signal charges (Q1 + Q2) and (Q1` + Q2`) are moved one line at a time from the CCD vertical shift register 2 to the horizontal shift register 3 and then they are sequentially transferred in the horizontal direction but fails to teach that the signal charges (Q1 + Q2) and (Q1` + Q2`) are compounded in the horizontal shift register originated from the portions

of vertical shift registers corresponding to each odd line into the information charges originated from the portions of vertical shift registers corresponding to each even line; and driving the horizontal shift register after compounding in the horizontal shift register to obtain an information output of the solid state imaging device.

However Murayama et al. teaches that charges from an odd row and an even number row are added in the horizontal transfer section 116 after no charge division (by setting w to 0) and then driving the horizontal shift register after compounding in the horizontal shift register to obtain an information output of the solid state imaging device (212) in order to minimize the flicker noise associated with an interlace scanning process used together with the frame signal store system (col. 5 line 36-col. 6 line 6).

Therefore taking the combined teachings of Hamasaki and Murayama, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have added the charges generated in the odd and even lines in the horizontal transfer section 116 after no charge division (by setting w to 0) and then driving the horizontal shift register after compounding in the horizontal shift register to obtain an information output of the solid state imaging device (212) in order to minimize the flicker noise associated with an interlace scanning process used together with the frame signal store system.

[Claim 2]

Hamasaki teaches that the duration of the second period is lesser than the first exposure period, which means lesser charges are generated during the second exposure period (col. 5 line 1).

[Claim 3]

Hamasaki also teaches that the second exposure time is a predetermined time (col. 5 line 1), therefore it would be inherent that the amount of information charges generated in a light receiving pixel corresponding to a maximum luminance portion of an object during the second period falls within a predetermined range relative to the charge storage capacity of the light receiving pixel.

[Claim 7]

Hamasaki teaches that the light receiving pixels are arranged in a matrix form (col. 3 line 60-64).

[Claim 8]

Hamasaki teaches in figures 4A and 4B that Q1 and Q2 are being independently vertically transferred from the pixels in the odd and even line.

[Claim 5]

See claim 2.

[Claim 6]

See claim 3.

[Claim 9]

See claim 7.

[Claim 10]

See claim 8.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 11-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Hamasaki (US Patent # 5,990,952).

[Claims 11 and 14]

Hamasaki teaches a method for driving a solid state imaging device (figure 1) comprising accumulating information charges generated in a plurality of light receiving pixels (figure 1, sensor 1) during a first period in portions of vertical shift registers (2) corresponding to each odd line and in portions of vertical shift registers corresponding to each even line (col. 4 lines 20-41, figure 2), vertically transferring the information charges (figure 4A, charge Q1 and Q2) accumulated in the portions of vertical shift registers (2) corresponding to each odd line to the portions of vertical shift registers corresponding to each adjacent even line, compounding the information charges (Q1 + Q2) originated from the portions of vertical shift registers corresponding to each odd line into the information charges accumulated in the portions of vertical shift registers corresponding to each adjacent even line, and holding resultant information charges in the portions of vertical shift registers corresponding to each even line (col. 4 lines 41- 67, Col. 5 lines 22-28, figures 4A, 4B and 4C),

accumulating information charges generated in a light receiving pixel in each odd line (Q1`) during a second period (figure 3 shows short exposure time) in the portions of vertical shift registers (2) corresponding to each odd line, and of accumulating information charges generated in a light receiving pixel in each even line (Q2`) during the second period in the portions of vertical shift registers corresponding to each even line in addition to the information charges that are already accumulated therein (col. 4 line 67- col. 5 line 21, col. 5 lines 29-30, figures 4A-4D);

transferring the information charges accumulated in the portions of vertical shift registers corresponding to each odd line and the information charges accumulated in the portions of vertical shift registers corresponding to each even line to a horizontal shift registers (col. 6 lines 25-37).

[Claims 12 and 15]

Hamasaki teaches that the duration of the second period is lesser than the first exposure period, which means lesser charges are generated during the second exposure period (col. 5 line 1).

[Claims 13 and 16]

Hamasaki also teaches that the second exposure time is a predetermined time (col. 5 line 1), therefore it would be inherent that the amount of information charges generated in a light receiving pixel corresponding to a maximum luminance portion of an object during the second period falls within a predetermined range relative to the charge storage capacity of the light receiving pixel.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K. Aggarwal whose telephone number is (571) 272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571)-272-7593. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YKA
August 15, 2005

DAVID L. OMETZ
SUPERVISORY PATENT
EXAMINER